> both a silicon nitride layer and a silicon oxide layer over the recited gate electrode. Specifically, in figure 1, a first interlayer insulating film 19 and a second interlayer insulating film 21, are sequentially formed over the gate electrodes 15 and 16, where as stated in col. 4, lines 65-68, col. 5, lines 6-10, the first and second interlayer insulating films are formed of either silicon nitride or silicon oxide. Therefore, since both interlayer insulating films include one of silicon nitride or silicon oxide materials the combination of an interlayer insulating film with a silicon nitride layer and a silicon oxide layer will be included within the combined first and second interlayer insulating films.

Page 7 of Office Action. Applicants submit that gate electrodes 15 and 16, referenced by the Examiner as having both a silicon nitride layer and a silicon oxide layer formed over them, are part of CMOS transistor 3 used in a *peripheral circuit*, not in an *active matrix circuit*. See, e.g., col. 3, lines 12-14. Rather, Matsumoto only discloses NMOS transistor 2, which has a gate electrode 20, as being used in a *matrix circuit*. See, e.g., col. 2, line 67 to col. 3, line 7 ("In the thin film semiconductor device shown in the drawing [Fig. 1], an NMOS thin film transistor 2 for a *matrix circuit* and a CMOS thin film transistor 3 for a *peripheral circuit* are formed at predetermined positions on the upper surface of an insulating substrate ..." (emphasis added)). Accordingly, the Examiner's reference to Matsumoto's description of forming a combination interlayer insulating film having a silicon nitride layer and a silicon oxide layer over gate electrodes 15 and 16 is not relevant insofar as this step is not part of a method of forming an *active matrix circuit*, as claimed.

As stated in the Response to the Office Action mailed on February 9, 2005, Matsumoto describes forming the NMOS thin film transistor 2 in the *matrix circuit* of the device by, in part, forming a second interlayer insulating film 21 over the gate electrode 20, which has been formed over a first interlayer insulating film 19. Thus, the interlayer insulating film 19 acts as a gate insulating film in the matrix circuit of the device and as an interlayer insulating film in the peripheral circuit of the device. See Fig. 2, col. 5, lines 4-10; 21-27. The second interlayer insulating film 21 that is formed over the gate electrode 20, however, does not include both a silicon nitride layer and a silicon oxide layer, as claimed. Rather, the second interlayer insulating film 21 is either a silicon oxide layer or a silicon nitride layer, but not both. See col. 5, lines 8-10.

Iwanaga describes a thin film semiconductor device including a thin film transistor having a thin film semiconductor on an insulation substrate to define an element region, and a hygroscopic interlayer dielectric which covers the element. Iwanaga, however, does not remedy

the deficiency of Matsumoto to describe or suggest forming an active matrix circuit by forming an interlayer insulating film that includes a silicon nitride layer and a silicon oxide layer over the recited gate electrode.

For at least these reasons, applicants request reconsideration and withdrawal of the rejection of claims 16, 22 and 28, and their dependent claims 17, 19-21, 23, 25-27, 29-31 and 33-36.

Claims 18, 24 and 32, which depend from claims 16, 22 and 28, respectively, have been rejected as being unpatentable over Matsumoto in view of Iwanaga and in further view of Shannon (U.S. Patent No. 5,466,617). Shannon does not remedy the failure of Matsumoto and Iwanaga to describe or suggest forming an active matrix circuit by forming an interlayer insulating film that includes a silicon nitride layer and a silicon oxide layer over the gate electrode. Accordingly, for at least the reasons described above, applicants request reconsideration and withdrawal of the rejection of claims 18, 24 and 32.

Applicants submit that all claims are in condition for allowance.

Please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 11/14/05

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